Cadence Conformal Lec User Manual

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Introducing Conformal Smart LEC Equivalence Checking / Formal Verification S-7 | Logic Equivalence Check using Formality | RTL-to-

GDSII flow | Synopsys Formality tutorial Conformal Mapping Lec 1 *Understanding Logic Equivalence Check in VLSI | What is LEC? JasperGold RTL Designer Signoff with Superlint and CDC -- Cadence Design Systems* **Very Basic Introduction to Formal Verification Rambus Automates ECOs and Saves Time with Cadence Conformal ECO Designer** *Broadcom Uses Conformal ECO for High-Performance Designs* LIB file | DB file | Verilog file | Description of various files used in VLSI Design | session-1 S-10 | Place and Route in Cadence Innovus | full PnR flow | Cadence

Innovus demo RTL to GDSII
flow | Introduction of RTL
to GDS Flow | Various EDA
tools used in RTL to GDS
flow From Sand to Silicon:
the Making of a Chip | Intel
*Filler Cells | Physical
Design Interview experience
at Synopsys COMPLETE ASIC
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DESIGN COMPILER (DESIGN
VISION) | PHYSICAL DESIGN |
VLSIFaB* CLOCK TREE SYNTHESIS
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*Introduction to Floor
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VLSIFaB ASIC Design flow*
What is Formal Verification?

An introduction to Formal Verification Part 1

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MEMS Design Course - Lecture 02

INVECAS' Smart Constraint and CDC Signoff with Cadence's Conformal Litmus

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Cadence Conformal Lec User Manual - ModApkTown At CDNLive Korea, Cadence announced the logical equivalence checking (LEC) would get smart. And not in the Maxwell Smart sense. It's about 20 times faster and doesn't require manual guidance (self-driving LEC). The new product is

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solution. Offering key
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improves runtime by an
average of 4X compared to
existing solutions with the
same compute resources.

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equivalence checking solution.

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Manager Refresh Window
Schematics . Title:
Microsoft PowerPoint -
conformal_debug Author:
NotNaeem Created Date:
5/4/2010 11:38:55 PM ...

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Conformal Smart Logic Equivalence Checker is the next-generation equivalency checking solution. With massively parallel architecture and adaptive proof technology, the Conformal Smart LEC delivers dramatic turnaround time improvements in equivalence checking by over 20X for RTL-to-gate comparisons.

Conformal Smart LEC - Cadence Design Systems

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Cadence®Conformal Smart LEC is the next-generation equivalence checking solution. Offering key technologies of massive parallelism and adaptive proof, Conformal Smart LEC improves runtime by an average of 4X compared to existing solutions with the same compute resources.

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Conformal ECOs at Marvell during pre-mask stage. We have done multiple ECOs using Conformal automated flow on various projects for the past few years. Below is the data for •Example 1 – Block A – Pre-mask ECO was done inside a control block which was instanced multiple(12) times. ECO fix involved combinational logic

change in control block.

Cadence Conformal suite of
tools contains a tool called
Logic Equivalence Checker or
LEC. Section 4 of this
tutorial describes how to
formally verify that the
synthesized design is
functionally equivalent to
the RTL description using
LEC. This section can be
skipped if one chooses to
use Formality for
equivalence checking.

Cadence Conformal EC enables

designers to verify the widest variety of circuits, including complex arithmetic logic, datapaths, memories, and custom logic. REQUEST INFORMATION . Already proven in thousands of tapeouts, Conformal EC is the industry's most widely supported independent equivalence checking product. It is production-proven on ...

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Guide

SAN JOSE, Calif. -- Sep 13,
2017 -- Cadence Design
Systems, Inc. (NASDAQ: CDNS)
today announced the Cadence®
Conformal® Smart Logic
Equivalence Checker (LEC),
the next-generation
equivalence checking
solution that delivers a
significant improvement in
equivalence checking runtime
with minimal user effort.
The Conformal Smart LEC
delivers an average of 4X
runtime improvement compared
to the previous generation
of logic equivalency
checking tools with the same
compute resources.

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